|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0000/0001/0010 | ALU Operations | 0011 | LHI | 0100 | LOAD |
| |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  S1  ALU PC | |  | | I6 – 8  A1RF  I9 – 11  A2RF  D1 E1  S2  D2 E2 | |  | | E1 ALU  E2 ALU  S3  ALU T1 | |  | | I3 – 5 A3RF  S37  T1 D3RF | |  | | PC D3RF  S4  “111” A3RF | | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC | |  | | I0 – 8  SE9 – 16  LS7  LS7  D3RF  S6  I9 – 11  A3RF | |  | | PC D3  S7  “111” A3RF |   S5 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  S8  ALU PC | |  | | I6 – 8  A1RF  S9  D1 E1 | |  | | E1 ALU  I0 – 5  SE6 – 16  ALU  S10  ALU T1 | |  | | T1 MEMDAT (A)  MEMDAT (DO) T2, D3RF  I9 – 11  A3RF | |  | | T2 ALU  0 ALU  PC D3  S12  “111” A3RF |   S11 | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0101 | STORE  S13 | 0110 | LOAD MULTIPLE  S17 | 0111 | STORE MULTIPLE  S22 |
| |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S14 | |  | | I6 – 8  A1RF  I9 – 11  A2RF  D1 E1  D2 E2  S15 | |  | | E1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1  S16 | |  | | T1 MEMDAT (A)  E2 MEMDAT(DI)  PC D3RF  “111” A3RF | | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S18 | |  | | I9-11  A2RF  D2 T1  I0-7  PEINPUT | |  | | do {T1 MEMDAT(A)  MEMDAT (DO) T2  S20 | |  | | T2 D3RF  PEOUTPUT A3RF  T1 ALU  +1 ALU  ALU T1}  while (! invalid\_next);  S21 | |  | | PC D3RF  “111” A3RF |   S19 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S23 | |  | | I9-11  A2RF  D2 T1  I0-7  PEINPUT  S24 | |  | | do {T1 T2  PEOUTPUT A1RF  D1RF E1  S25 | |  | | T2 MEMDAT(A)  E1MEMDAT(DI)  T1 ALU  +1 ALU  ALU T1  while (! invalid\_next);  S26 | |  | | PC D3RF  “111” A3RF | | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1100 | BEQ  S27 | 1000 | JAL  S31 | 1001 | JLR  S34 |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S28 | | |  | |  | | | | | |  | I6 – 8  A1RF  I9 – 11  A2RF  D1 EQU  D2 EQU | | |  | | S30  S29 | | | | | | PC D3RF  “111” A3RF | |  | T1 D3RF  “111” A3RF | | | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S32 | |  | | R7 D3RF  I9-11 A3RF  R7 ALU  I0 – 8  SE9 – 16  ALU  ALU PC | |  | | PC D3RF  “111” A3RF |   S33 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC | |  | | I6 – 8  A1RF  D1RF PC  I9 – 11  A3RF  R7 D3RF  S36 | |  | | PC D3RF  “111” A3RF |   S35 | |

# State Merging and Equivalence

//Note: S12 will require an additional signal from the Instruction Decoder. It differs from the other states in one input to the ALU. Can be modelled as a multiplexer. Also only S2 must cause a change in the flags. //

This leaves us with 16 states in total.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0000/0001/0010 | ALU Operations | 0011 | LHI | 0100 | LOAD |
| |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  S1  ALU PC | |  | | I6 – 8  A1RF  I9 – 11  A2RF  D1 E1  S2  D2 E2 | |  | | E1 ALU  E2 ALU  S3  ALU T1 | |  | | I3 – 5 A3RF  T1 D3RF | |  | | PC D3RF  S5  “111” A3RF |   S4 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC | |  | | I0 – 8  SE9 – 16  LS7  LS7  D3RF  S6  I9 – 11  A3RF | |  | | PC D3  S5  “111” A3RF |   S1 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  S1  ALU PC | |  | | I6 – 8  A1RF  S2  D1 E1 | |  | | E1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1 | |  | | T1 MEMDAT (A)  MEMDAT (DO) T2, D3RF  I9 – 11  A3RF | |  | | T2 ALU  0 ALU  PC D3  “111” A3RF |   S8  S7  S5 | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0101 | STORE  S1 | 0110 | LOAD MULTIPLE  S1 | 0111 | STORE MULTIPLE  S1 |
| |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S2 | |  | | I6 – 8  A1RF  I9 – 11  A2RF  D1 E1  D2 E2 | |  | | E1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1  S9 | |  | | T1 MEMDAT (A)  E2 MEMDAT(DI)  PC D3RF  “111” A3RF |   S7 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S2 | |  | | I9-11  A2RF  D2 T1  I0-7  PEINPUT | |  | | do {T1 MEMDAT(A)  MEMDAT (DO) T2  S11 | |  | | T2 D3RF  PEOUTPUT A3RF  T1 ALU  +1 ALU  ALU T1}  while (! invalid\_next);  S5 | |  | | PC D3RF  “111” A3RF |   S10 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S2 | |  | | I9-11  A2RF  D2 T1  I0-7  PEINPUT  S12 | |  | | do {PEOUTPUT A2RF  D2RF E2  S13 | |  | | T1 MEMDAT(A)  E2MEMDAT(DI)  T1 ALU  +1 ALU  ALU T1  while (! invalid\_next);  S5 | |  | | PC D3RF  “111” A3RF | | |
|  | |  | |  | |
|  | |  | |  | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1100 | BEQ  S1 | 1000 | JAL  S1 | 1001 | JLR  S1 |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S2 | | |  | |  | | | | | |  | I6 – 8  A1RF  I9 – 11  A2RF  D1 EQU  D2 EQU | | |  | | S5  S14 | | | | | | PC D3RF  “111” A3RF | |  | R7 ALU  I0 – 5  SE6 – 16  ALU  ALU PC | | |  | |  |  | | |  | |  | PC D3RF  “111” A3RF | |   S5 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC  S15 | |  | | PC D3RF  I9-11 A3RF  R7 ALU  I0 – 8  SE9 – 16  ALU  ALU PC | |  | | PC D3RF  “111” A3RF |   S5 | | |  | | --- | | R7 MEMINS (A)  MEMINS (D) IR  R7 ALU  +1 ALU  ALU PC | |  | | I6 – 8  A1RF  D1RF PC  I9 – 11  A3RF  PC D3RF  S5 | |  | | PC D3RF  “111” A3RF |   S16 | |